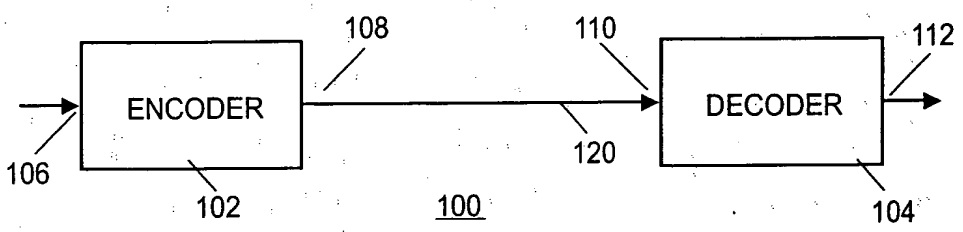
ENCODER
DECODER
106
102
108
110
120
112
104
100

FIG. 1

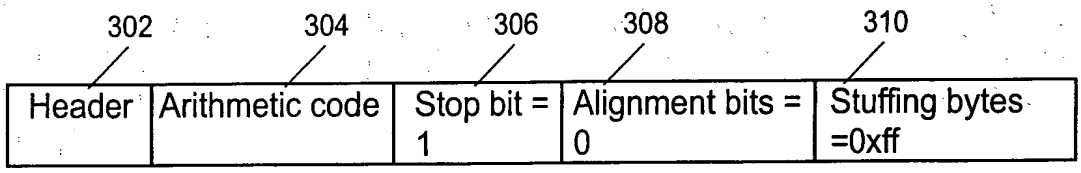
302
304
306
308
310
Header
Arithmetic code
Stop bit = 1
Alignment bits = 0
Stuffing bytes =0xff
300

FIG. 3

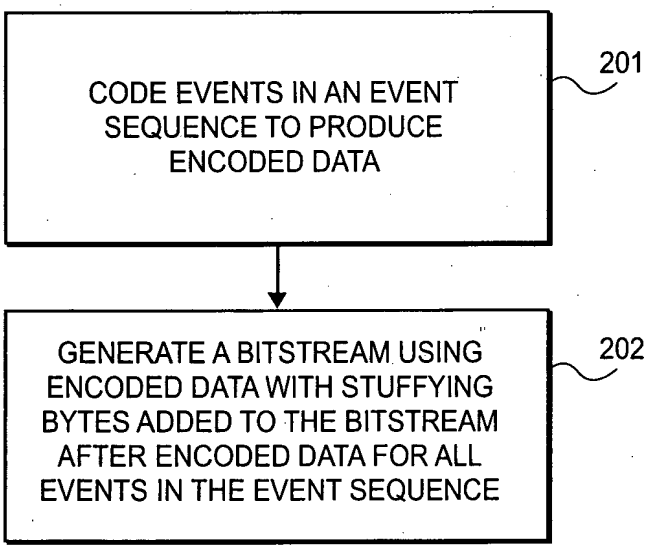
CODE EVENTS IN AN EVENT SEQUENCE TO PRODUCE ENCODED DATA
201
GENERATE A BITSTREAM USING ENCODED DATA WITH STUFFYING BYTES ADDED TO THE BITSTREAM AFTER ENCODED DATA FOR ALL EVENTS IN THE EVENT SEQUENCE
202

FIG. 2

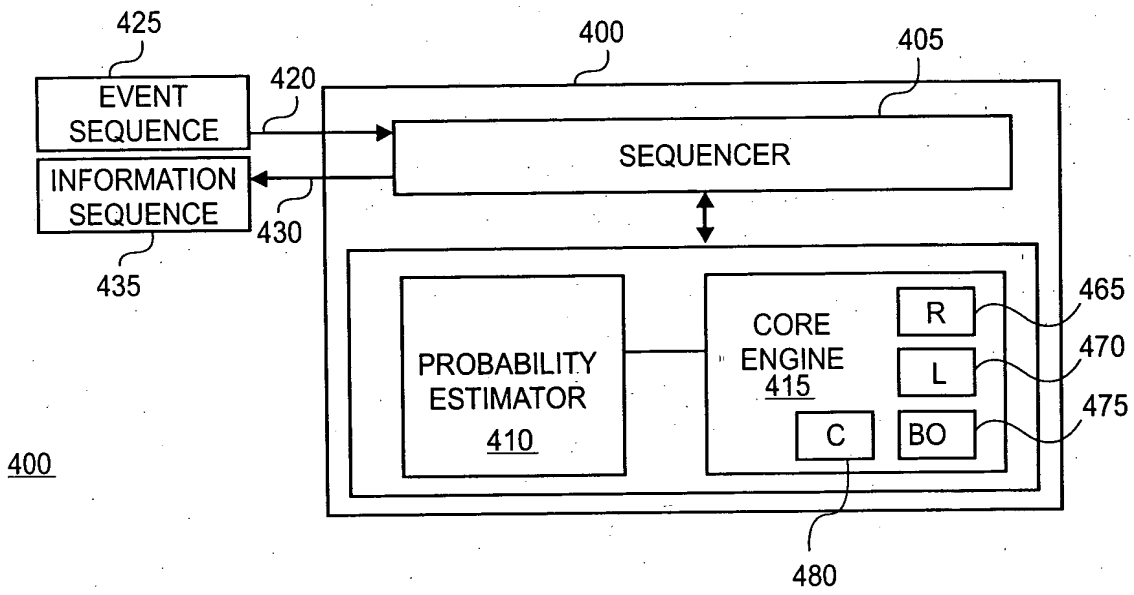
425
EVENT SEQUENCE
420
INFORMATION SEQUENCE
430
435
400
405
SEQUENCER
PROBABILITY ESTIMATOR
410
CORE ENGINE
415
R
L
C
BO
465
470
475
480
400

FIG. 4

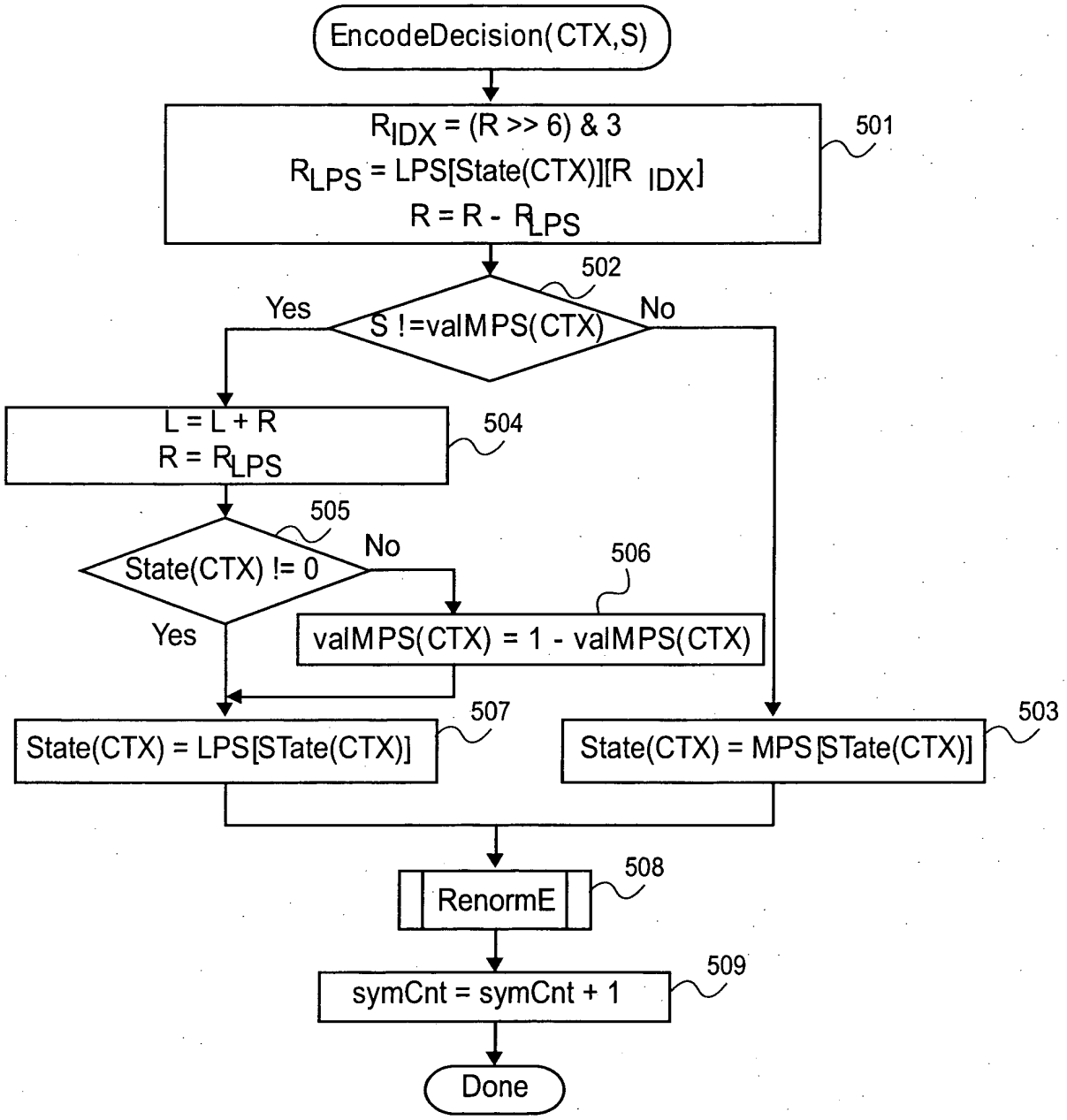
EncodeDecision(CTX,S)
$R_{IDX} = (R >> 6) \& 3$
$R_{LPS} = LPS[State(CTX)][R_{IDX}]$
$R = R - R_{LPS}$
501
502
Yes
S !=valMPS(CTX)
No
L = L + R
$R = R_{LPS}$
504
505
State(CTX) != 0
No
506
Yes
valMPS(CTX) = 1 - valMPS(CTX)
507
State(CTX) = LPS[STate(CTX)]
503
State(CTX) = MPS[STate(CTX)]
508
RenormE
509
symCnt = symCnt + 1
Done

FIG. 5

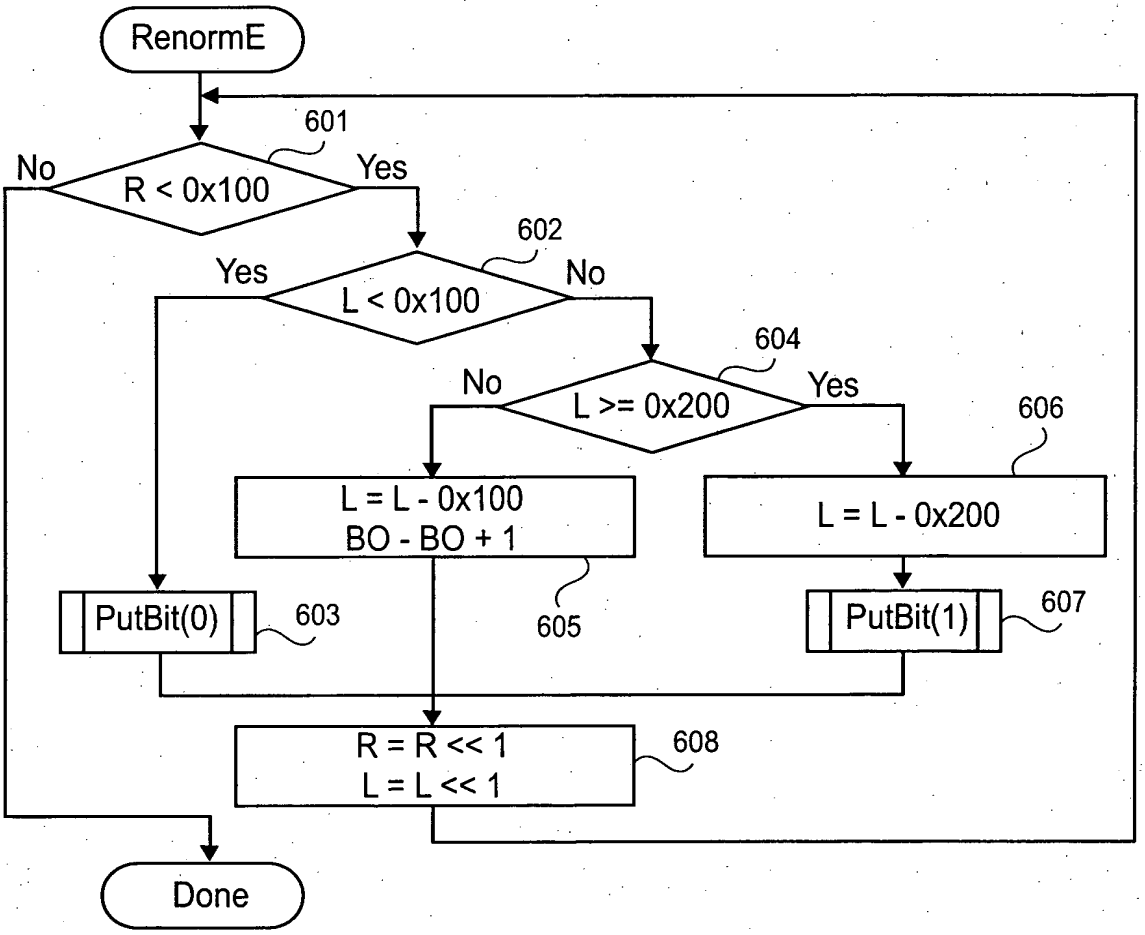
RenormE
601
No
R < 0x100
Yes
602
Yes
L < 0x100
No
604
No
L >= 0x200
Yes
606
L = L - 0x100
BO - BO + 1
L = L - 0x200
PutBit(0)
603
605
PutBit(1)
607
R = R << 1
L = L << 1
608
Done

FIG. 6

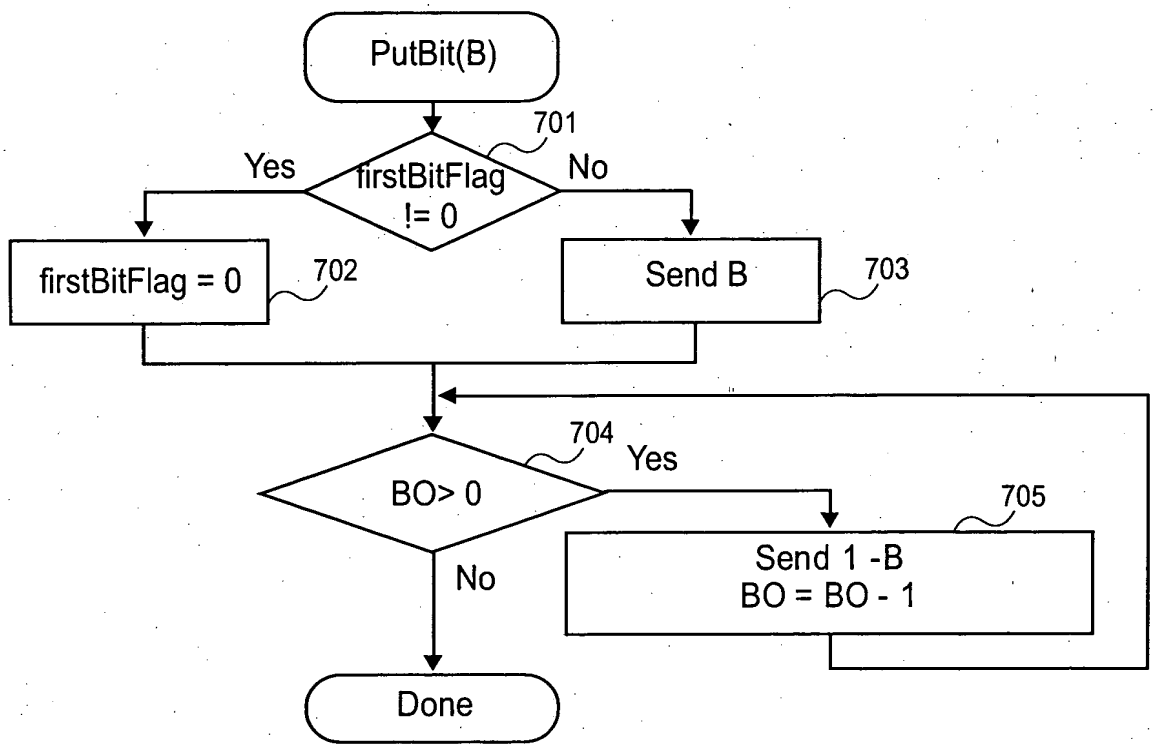
PutBit(B)
701
firstBitFlag
!= 0
Yes
No
firstBitFlag = 0
702
Send B
703
704
BO> 0
Yes
705
Send 1 -B
BO = BO - 1
No
Done

FIG. 7

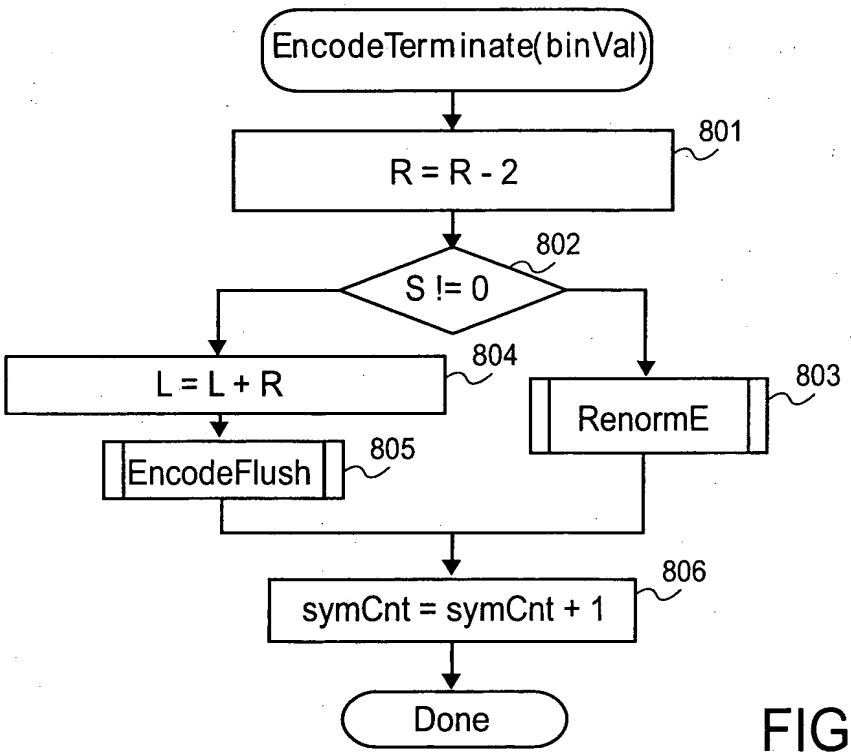
EncodeTerminate(binVal)
801
R = R - 2
802
S != 0
804
L = L + R
803
RenormE
805
EncodeFlush
806
symCnt = symCnt + 1
Done

FIG. 8

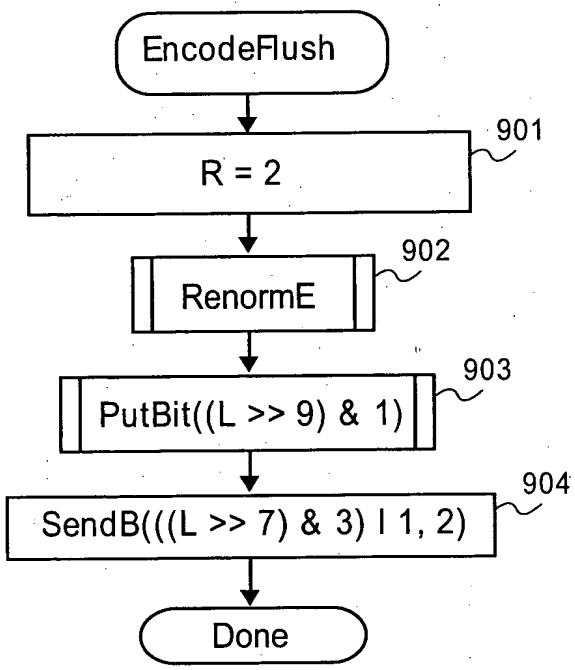
EncodeFlush
R = 2
901
RenormE
902
PutBit((L >> 9) & 1)
903
SendB(((L >> 7) & 3) | 1, 2)
904
Done

FIG. 9

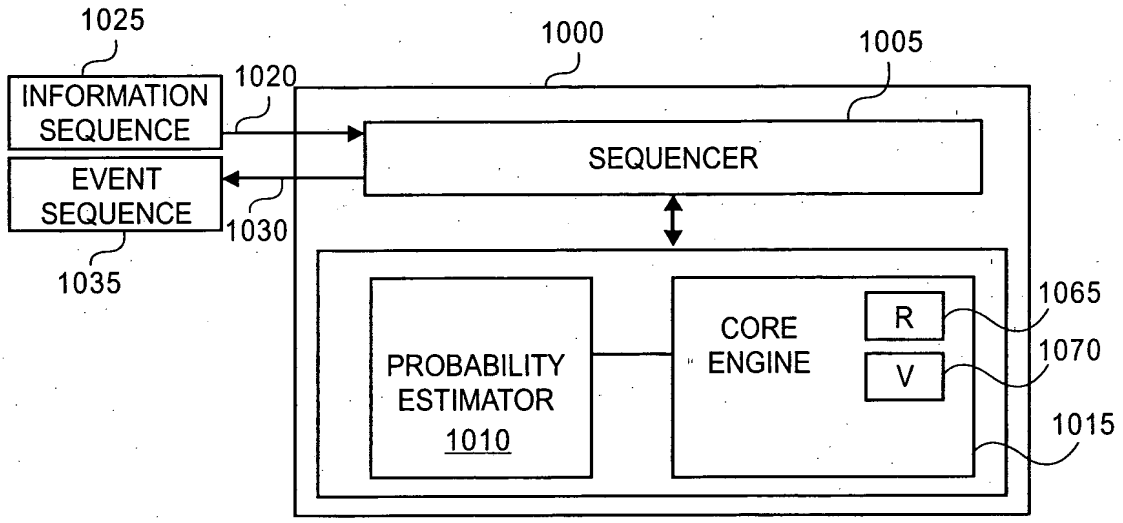
1025
INFORMATION SEQUENCE
1020
EVENT SEQUENCE
1030
1035
1000
1005
SEQUENCER
PROBABILITY ESTIMATOR
1010
CORE ENGINE
R
V
1065
1070
1015

FIG. 10

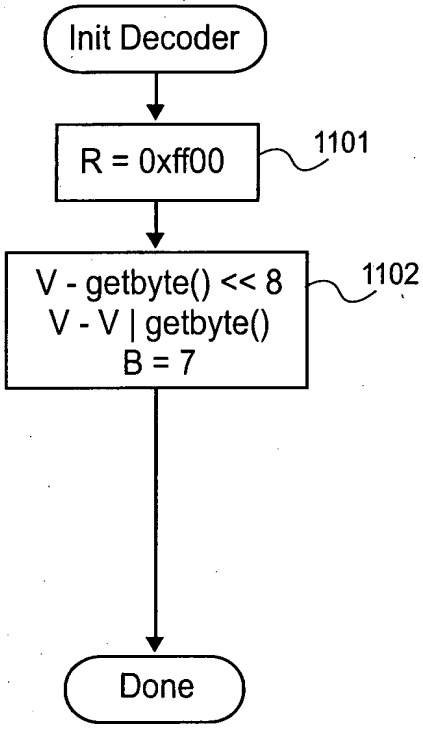
Init Decoder
R = 0xff00
1101
V - getbyte() << 8
V - V | getbyte()
B = 7
1102
Done

FIG. 11

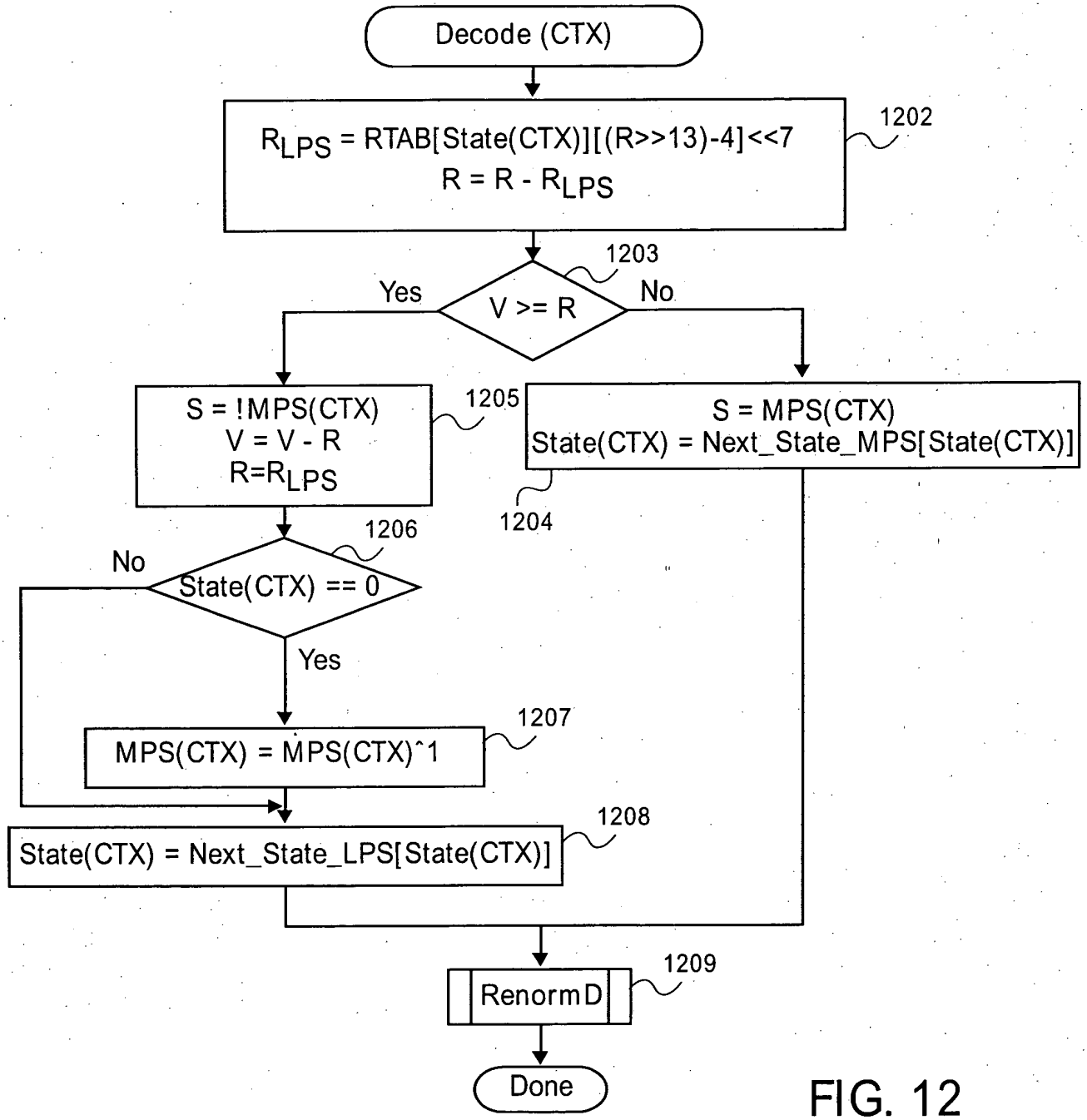
Decode (CTX)
R_{LPS} = RTAB[State(CTX)][(R>>13)-4]<<7
R = R - R_{LPS}
1202
1203
Yes
V >= R
No
S = !MPS(CTX)
V = V - R
R=R_{LPS}
1205
S = MPS(CTX)
State(CTX) = Next_State_MPS[State(CTX)]
1204
1206
No
State(CTX) == 0
Yes
MPS(CTX) = MPS(CTX)^1
1207
State(CTX) = Next_State_LPS[State(CTX)]
1208
RenormD
1209
Done

FIG. 12

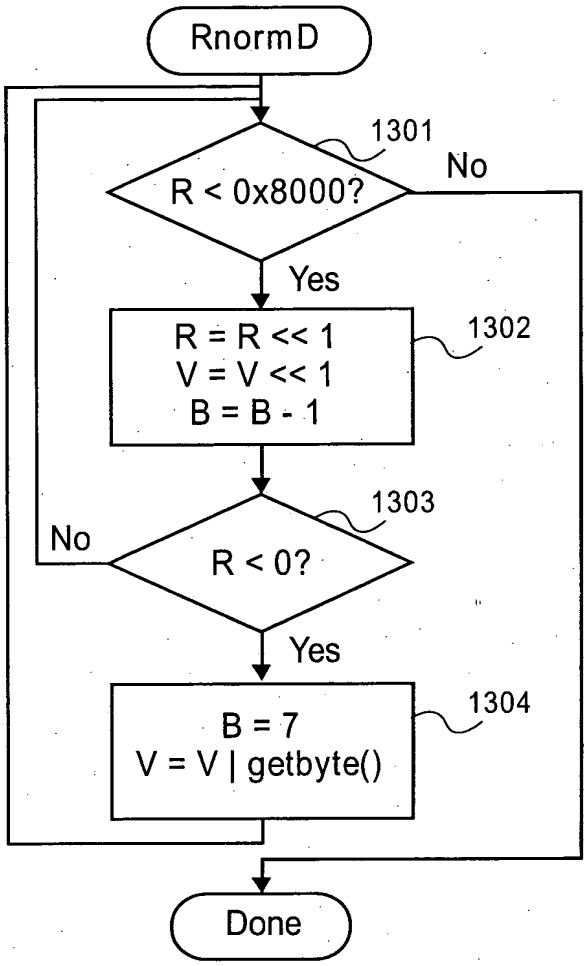
RnormD
1301
R < 0x8000?
No
Yes
R = R << 1
V = V << 1
B = B - 1
1302
1303
No
R < 0?
Yes
B = 7
V = V | getbyte()
1304
Done

FIG. 13

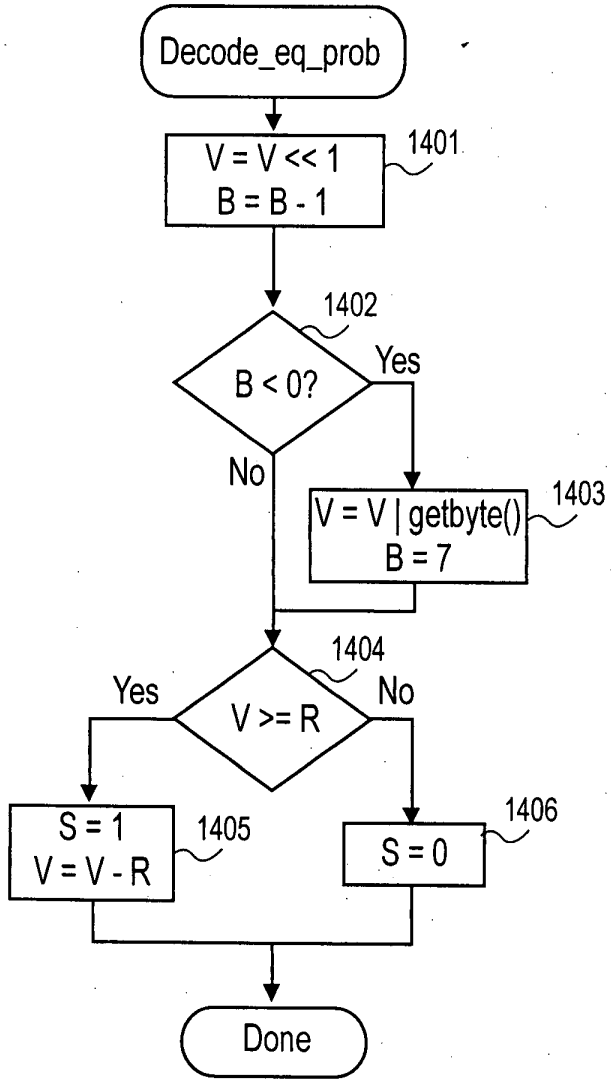

FIG. 14A

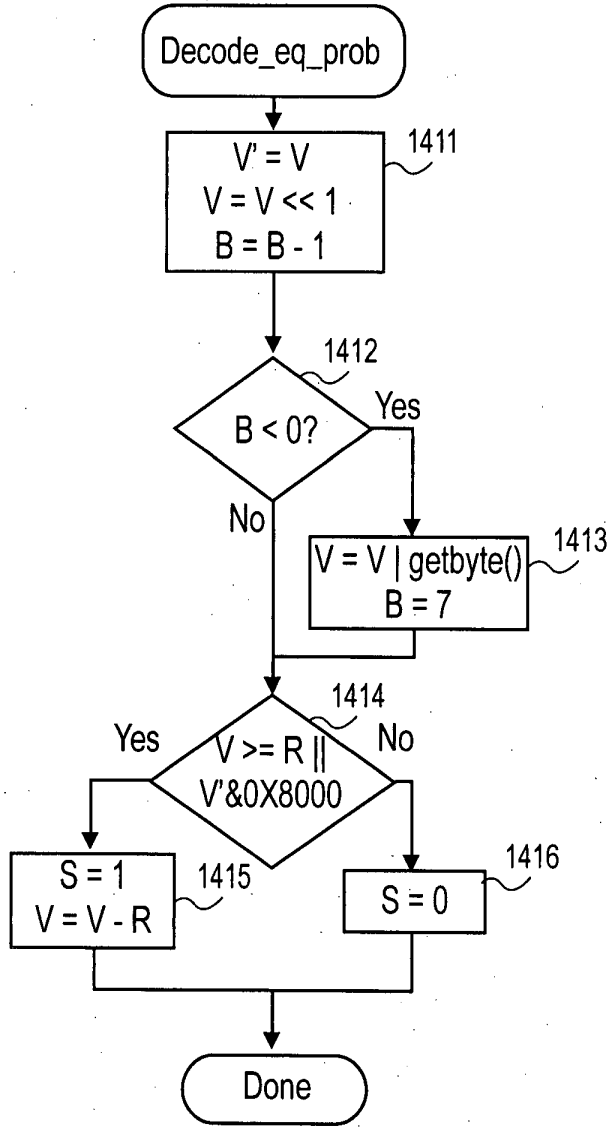

FIG. 14B

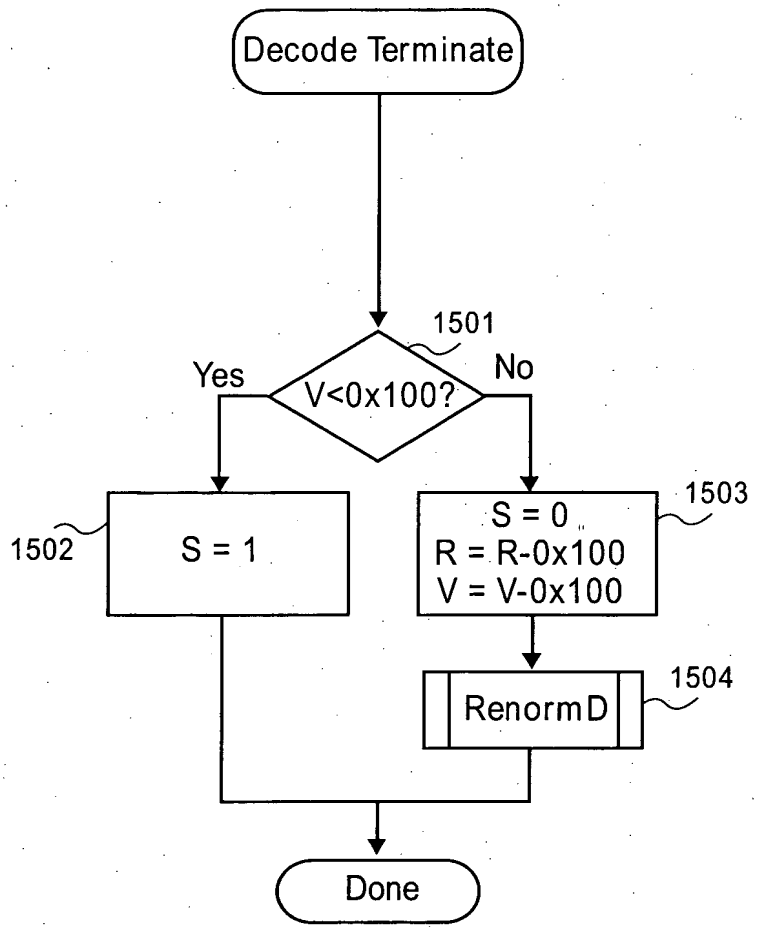
Decode Terminate
1501
Yes
V<0x100?
No
1502
S = 1
S = 0
R = R-0x100
V = V-0x100
1503
RenormD
1504
Done

FIG. 15A

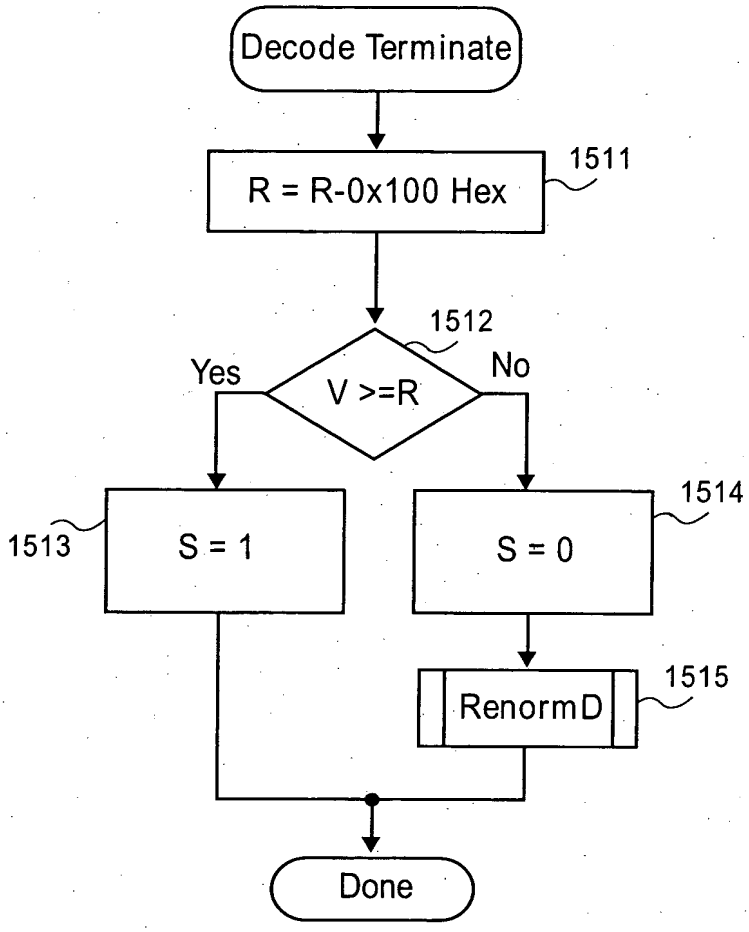
Decode Terminate
R = R-0x100 Hex
1511
1512
V >=R
Yes
No
1513
S = 1
S = 0
1514
RenormD
1515
Done

FIG. 15B

State (CTX)	R_{IDX}				State (CTX)	R_{IDX}			
	0	1	2	3		0	1	2	3
0	128	176	208	240	32	27	33	39	45
1	128	167	197	227	33	26	31	37	43
2	128	158	187	216	34	24	30	35	41
3	123	150	178	205	35	23	28	33	39
4	116	142	169	195	36	22	27	32	37
5	111	135	160	185	37	21	26	30	35
6	105	128	152	175	38	20	24	29	33
7	100	122	144	166	39	19	23	27	31
8	95	116	137	158	40	18	22	26	30
9	90	110	130	150	41	17	21	25	28
10	85	104	123	142	42	16	20	23	27
11	81	99	117	135	43	15	19	22	25
12	77	94	111	128	44	14	18	21	24
13	73	89	105	122	45	14	17	20	23
14	69	85	100	116	46	13	16	19	22
15	66	80	95	110	47	12	15	18	21
16	62	76	90	104	48	12	14	17	20
17	59	72	86	99	49	11	14	16	19
18	56	69	81	94	50	11	13	15	18
19	53	65	77	89	51	10	12	15	17
20	51	62	73	85	52	10	12	14	16
21	48	59	69	80	53	9	11	13	15
22	46	56	66	76	54	9	11	12	14
23	43	53	63	72	55	8	10	12	14
24	41	50	59	69	56	8	9	11	13
25	39	48	56	65	57	7	9	11	12
26	37	45	54	62	58	7	9	10	12
27	35	43	51	59	59	7	8	10	11
28	33	41	48	56	60	6	8	9	11
29	32	39	46	53	61	6	7	9	10
30	30	37	43	50	62	6	7	8	9
31	29	35	41	48	63	2	2	2	2

FIG. 16A

State(CTX)	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
transIdxLPS	0	0	1	2	2	4	4	5	6	7	8	9	9	11	11	12
transIdxMPS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
State(CTX)	**16**	17	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
transIdxLPS	13	13	15	15	16	16	18	18	19	19	21	21	22	22	23	24
transIdxMPS	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
State(CTX)	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**
transIdxLPS	24	25	26	26	27	27	28	29	29	30	30	30	31	32	32	33
transIdxMPS	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
State(CTX)	**48**	**49**	**50**	**51**	**52**	**53**	**54**	**55**	**56**	**57**	**58**	**59**	**60**	**61**	62	**63**
transIdxLPS	33	33	34	34	35	35	35	36	36	36	37	37	37	38	38	63
transIdxMPS	49	50	51	52	53	54	55	56	57	58	59	60	61	62	62	63

FIG. 16B

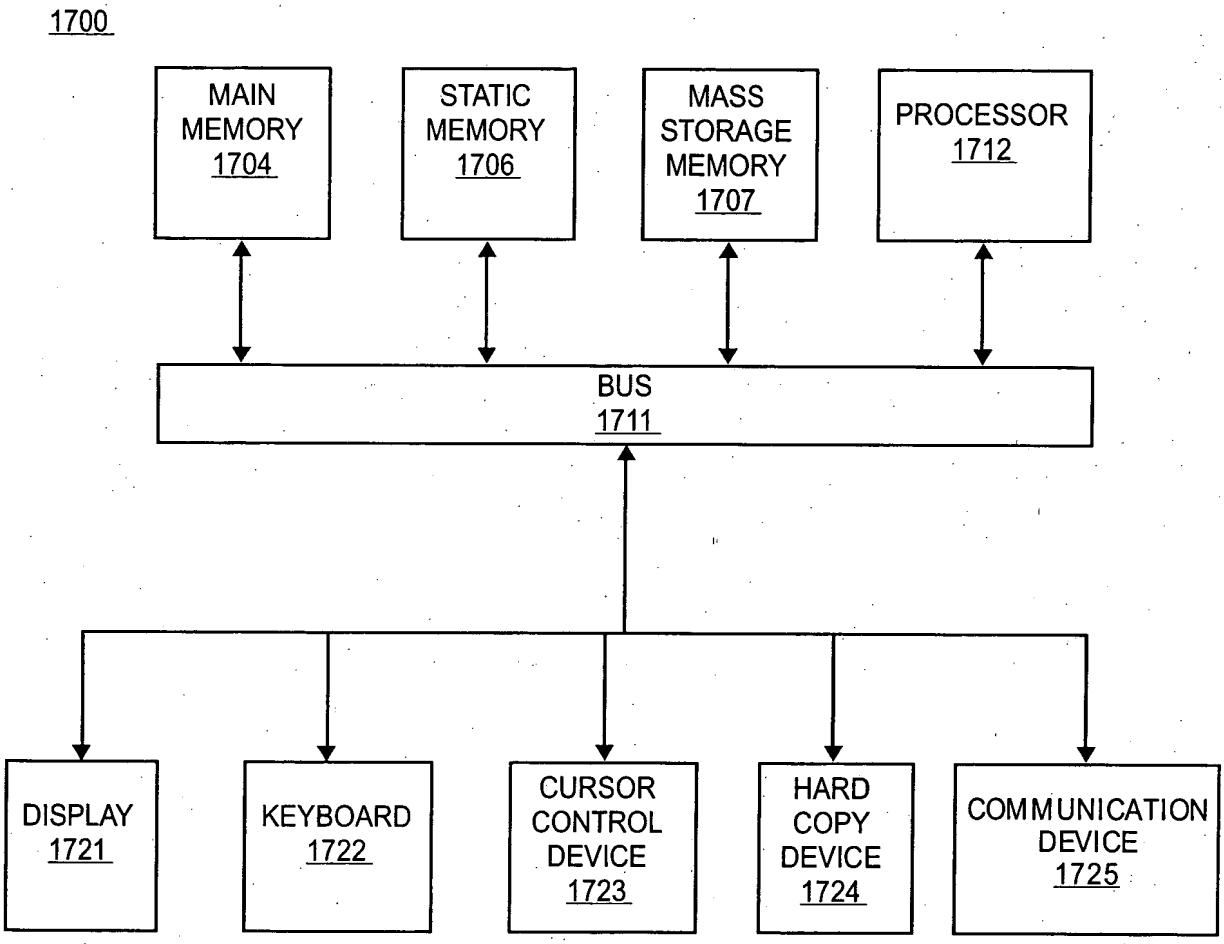
1700
MAIN MEMORY 1704
STATIC MEMORY 1706
MASS STORAGE MEMORY 1707
PROCESSOR 1712
BUS 1711
DISPLAY 1721
KEYBOARD 1722
CURSOR CONTROL DEVICE 1723
HARD COPY DEVICE 1724
COMMUNICATION DEVICE 1725

FIG. 17